ABSTRACT OF THE DISCLOSURE

A procedure for translating ARM instructions of a first set into instructions of a second set for execution on an LX processor comprising a core provides a first set of registers corresponding to the ARM instructions and a second set of registers corresponding to the instructions that can be executed on the LX processor. Each register of the first set is mapped in a corresponding register of the second set designed to emulate the behavior of the first register, obtaining a unique independent translation of the first set into the second set. The translation is performed by a translation device external to the LX core without altering the core, and the translation operating without accessing resources of the core, by the translating device intercepting accesses of the core to the storage area reserved to the ARM instructions.